AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An apparatus comprising:

an error detection component to control the detection of errors in information stored in a processor resource between stores of new information in the processor resource; and

a comparison component coupled to the error detection component, the comparison component to receive the information from the processor resource, to determine whether the information is valid, and to output a signal to indicate an error condition if the information is invalid, wherein the processor resource is selected from at least the group comprising a cache, at least one translation lookaside buffer (TLB), at least one region identification (RID), at least one protection key register, at least one model specific register (MSR), a control register access bus (CRAB) including at least one MSR coupled to the CRAB, a CRAB coupled to at least one other CRAB, and a TLB coupled to a MSR which is coupled to a CRAB.

2. (Previously Presented) The apparatus of claim 1, wherein the error detection component, comprises:

an error detection state machine (EDSM) to output a next-entry-to read-out signal and a parity bit signal.

3. (Previously Presented) The apparatus of claim 2, wherein the EDSM, comprises:

a timer to periodically output a next-entry-to-read-out signal to the processor resource;

a next pointer coupled to the timer, the next pointer to contain a pointer value, which specifies a specific piece of information to be read out from the processor resource;

a move-to-processor-resource logic component coupled to the timer, the move-to-processor-resource logic component to prevent the next-entry-to-read-out signal from being sent by the timer, if information is being moved into the processor resource;

a counter coupled to the move-to-processor-resource logic component, the counter to count the number of shifts needed to compute the parity bit; and

a parity and valid bits register coupled to the counter, the parity and valid bits register being configured to store at least one valid bit and parity bit pair.

4. (Previously Presented) The apparatus of claim 1, wherein the comparison component, comprises:

a shift register, the shift register to receive the processor resource information and to output a parity bit for the processor resource information;

a first exclusive OR (XOR) gate coupled to the shift register, the first XOR gate to receive the parity bit and a feedback signal and to output an indication of the validity of the parity bit; and

a second XOR gate coupled to the first XOR gate, the second XOR gate to receive the parity bit signal and the indication of the validity of the parity bit and to output a machine check abort (MCA) if the parity bit signal and the indication of the validity of the parity bit indicate the processor resource information is invalid.

5. (Previously Presented) The apparatus of claim 4 further comprising

a result latch coupled between the first XOR gate and the second XOR gate, the result

latch to receive the indication of the validity of the parity bit from the first XOR gate, and to output a polarized signal, which indicates the validity of the parity bit.

6. (Previously Presented) The apparatus of claim 5, wherein the first XOR gate is to receive the polarized signal as the feedback signal.

7. (Previously Presented) The apparatus of claim 5, wherein the result latch is further to transmit the polarized signal to the error detection component.

8. (Cancelled)

9. (Currently Amended) The apparatus of claim [[~~8~~]] 1, wherein the CRAB further comprises a checksum component coupled to the CRAB.

10. (Currently Amended) The apparatus of claim [[~~8~~]] 1, wherein the CRAB further comprises:

at least one MSR coupled to the CRAB; and

a checksum component coupled to the CRAB.

11. (Previously Presented) A method comprising:

controlling detection of errors in information stored in a processor resource, said controlling detection of errors including

requesting information from the processor resource by periodically outputting a next-entry-to-read-out signal to the processor resource, when information is not being moved into the processor resource;

computing a parity bit value for the information;

outputting the computed parity bit value to a comparison component;

comparing the computed parity bit value with an existing parity bit value associated with the information; and

outputting a signal to indicate an error condition, if the computed parity bit value is not equal to the existing parity bit value.

12. (Previously Presented) The method of claim 11, further comprising:

counting the number of shifts needed to compute the parity bit value.

13. (Previously Presented) The method of claim 11, wherein outputting a next-entry-to-read out signal comprises:

receiving a periodic read authorization signal;

determining if the processor resource is in use; and

outputting a next-pointer value indicating which item of information is to be read out, if the processor is not in use.

14. (Previously Presented) The method of claim 11, wherein computing the parity bit value, comprises:

receiving the information;

shifting-out the individual bits comprising the information; and

computing a parity bit value for the information.

15. (Withdrawn) The method of claim 11, wherein outputting a signal to indicate an error condition occurs if the computed parity bit value is different from the existing parity bit value.

16. (Previously Presented) The method of claim 11, wherein outputting a signal to indicate an error condition, comprises:

outputting a machine check abort (MCA) signal.

17. (Previously Presented) An article of manufacture comprising a machine-readable storage medium having stored thereon a plurality of executable instructions to perform a method comprising:

controlling detection of errors in information stored in a processor resource, said controlling detection of information including

requesting information from the processor resource by periodically outputting a next-entry-to-read-out signal to the processor resource, when information is not being moved into the processor resource;

computing a parity bit value for the information;

outputting the computed parity bit value to a comparison component;

comparing the computed parity bit value with an existing parity bit value

associated with the information; and

outputting a signal to indicate an error condition, if the computed parity bit value is not equal to the existing parity bit value.

18. (Previously Presented) The article of manufacture of claim 17, wherein the method further comprises:

counting the number of shifts needed to compute the parity bit value.

19. (Previously Presented) The article of manufacture of claim 17, wherein outputting a next-entry-to-read out signal comprises:

receiving a periodic read authorization signal;

determining if the processor resource is in use; and

outputting a next-pointer value indicating which item of information is to be read out, if the processor is not in use.

20. (Previously Presented) The article of manufacture of claim 17, wherein computing a parity bit value, comprises:

receiving the information;

shifting-out the individual bits comprising the information; and

computing a parity bit value for the information.

21. (Withdrawn) The article of manufacture of claim 17, wherein outputting a signal to indicate an error condition occurs if the computed parity bit value is different than the existing parity bit value.

22. (Original) The article of manufacture of claim 17, wherein outputting a signal to indicate an error condition, comprises:

outputting a machine check abort (MCA) signal.